Tunable Planar Capacitor

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Related Applications

This application claims the benefit of U.S. Provisional Application 60/283,093, filed April 11, 2001, which is hereby incorporated by reference. In addition, this application relates to U.S. Applications 09/904,631, "Tunable Ferro-Electric Filter," filed on July 13, 2001; 09/912,753, "Tunable Ferro-Electric Multiplexer," filed on July 24, 2001; 09/927,732, "Low Loss Tunable Ferro-electric Device and Method of Characterization," filed on August 8, 2001; and 09/927,136, "Tunable Matching Circuit," filed on August 10, 2001, which are hereby incorporated by reference.

BACKGROUND

Description of Related Art

Capacitors are commonly used in filters for wireless communication. Capacitors with capacitances in the range of 0.5 to 10.0 pF are typically employed in radio frequency signal paths to set resonant frequencies of filters to specific values. Additionally, capacitors are typically employed in

matching circuits to match impedances between components in wireless communication devices. A capacitor, in fact, is a fundamental component in electrical circuit design. As is well known in the art, capacitors can be found in many circuits throughout electronic industries and wherever electronic circuits are required.

Referring specifically to filters for use in wireless communication devices, related application number 09/904,631, discloses a tunable capacitor that has been developed for tuning the resonant frequency of a filter for use at different frequencies. Tunability can be achieved by applying a variable bias electric field to a ferro-electric (FE) material located in the field induced by the capacitor. FE materials have a dielectric constant that varies with the bias electric field. As the dielectric constant varies, the capacitance of the capacitor varies. This changes the resonant frequency of the filter.

As disclosed in patent application number 09/904,631, there are three basic types of capacitors in common use: gap capacitors, overlay capacitors and interdigital capacitors. Gap capacitors and

interdigital capacitors are both planar structures. That is, both electrodes of the capacitors are in the same plane. Overlay capacitors have electrodes that are in different planes, that is, planes that overlay each other. Typically, overlay capacitors can develop higher capacitances, but they are harder to fabricate than planar capacitors. Thus, this invention is focused on improving the biasing scheme for planar capacitors. The discussion below is directed to gap capacitors, but it will be understood that the methods and devices described herein apply equally to all planar capacitors.

It has proven difficult to apply the variable electric field to the FE material in RF applications without introducing (1) increased loss, (2) circuit complexity or (3) circuit size, or a combination of these three. The variable electric field is applied by applying a variable DC voltage to the FE material. Typically, in a planar capacitor, FE material is placed between the electrodes of the capacitor and the substrate. Thus, the FE layer is formed on the substrate. The capacitor electrodes are formed on the FE layer, with a gap between the electrodes, forming the capacitor.

One way of applying the DC voltage is to connect the DC voltage source to an electrode of the capacitor through a resistor. Often, a DC blocking capacitor must be used in the RF signal path so as to provide an RF ground for example, to the f-e capacitor without shorting out the dc bias applied.. The DC blocking capacitor invariably introduces added loss into the RF signal. This increased loss results in a lower signal to noise ratio for receive applications, which results in dropped communications, and increased power consumption in transmit applications, among other things. Additionally, the resistor and the DC blocking capacitor add to the cost, size and complexity of the device that the capacitor is used in. Thus, this method of applying the variable DC electric field to the FE material is not an optimal solution.

While planar f-e capacitors are relatively simple to fabricate, they require a larger DC bias voltage to tune, as the gap dimensions are necessarily large (typically greater than or equal to 2.0 microns) due to conventional patterning constraints. Overlay f-e capacitors, alternatively, can be tuned with a minimum DC voltage, as the plate separation can be made quite small (about 0.1 micron f-e film thickness is possible

and greater than about 0.25 microns is typical). Thus, the required DC bias field strength can be a factor of 20 to 40 times smaller for an overlay capacitor than for a gap capacitor. Furthermore, most all of the dc bias field is constrained within the f-e film in an overlay capacitor. This is not true in a gap or interdigital capacitor, where a significant portion of the dc bias field is located outside of the f-e film.

One significant problem with overlay capacitors is that they are more difficult to fabricate than gap capacitors, as they are multi-layer structures. They typically need a common bottom electrode on which the desired f-e thin film is deposited. Ideally the desired metals for the bottom electrodes are typically the low loss noble metals like gold, silver or preferably copper. The deposition requirements for most f-e films however, would cause the unacceptable formation of metal oxides. To prevent unwanted oxidation, the deposition of a high refractory metal, such as platinum as a cap, or covering, layer is needed, which adds an extra mask or layer as well as increases cost. Additionally, the bottom layer metal thickness should be increased to greater than about 2.0 skin depths, to minimize the metal loss in the bottom electrode.

Rather than relying on overlay capacitors, a compromise solution is to introduce a pair of bias electrodes into the vicinity of the gap of a planar capacitor. One version would pattern one bias electrode in the gap itself and place the other electrode between the substrate and the f-e layer. The variable DC electric field is applied to the FE material by putting bias electrodes in the form of doped silicon on both sides of the FE material. Thus, a first doped silicon layer is formed on the substrate. A FE layer is formed on the first doped silicon layer. The capacitor electrodes are formed on the FE layer. A second doped silicon layer is formed inside the gap region of the capacitor. The bias voltage is applied to the second doped silicon layer and the first doped silicon layer is grounded, or vice versa. This approach is not preferred, as it requires the presence of two bias electrodes, one above and one below the f-e layer as well as the presence of a bias electrode between the two rf electrodes in the gap capacitor.

Further, the gap typically must be widened to make room for the bias electrode between the two RF (capacitor) electrodes. Widening the gap reduces the capacitance of the structure. To bring the capacitance

back to a useful level, the capacitor must be made wider. This increases the size and cost of the capacitor. Additionally, it is difficult and costly to manufacture a gap capacitor with a conducting layer of doped silicon in the gap, since one must provide added grounding as well as bias for a two layer bias scheme.

Accordingly, it would be beneficial to have a tunable FE capacitor with a less complex, cheaper and smaller bias scheme for applying the variable DC electric field to the FE material in a planar tunable capacitor.

SUMMARY

Variable capacitors using a variable DC voltage to tune the capacitance typically employ costly and overly large components to apply the variable DC voltage to the capacitor. Furthermore, at least one method of applying the variable DC voltage in the prior art introduces added signal loss into the RF signal path due to the need for a DC blocking capacitor.

Thus, it is an object of the present invention to provide methods and devices for applying a variable DC voltage to a tunable capacitor which introduce lower loss, lower cost and are smaller than those methods and

devices previously available.

A bias electrode is positioned near a FE material. The capacitor electrodes are also positioned near the FE material, such that the capacitor electrodes and the bias electrode are not touching. There are only non-conductive materials, including possibly air, in the gap formed between the capacitor electrodes. The bias electrode is used to apply a variable DC voltage to the FE material. In a wide range of useful instances, one or both capacitor electrodes serve as a DC ground for producing a variable DC field between the bias electrode and the capacitor electrodes, thus eliminating the need for the extra DC blocking capacitor. Alternatively, one of the capacitor electrodes can be biased to, among other reasons, provide a modified capacitive response in that electrode. In other words, a single bias underlay electrode is added to a planar capacitor to achieve the biasing of the FE material. This allows for the elimination of biasing from either capacitor electrode. Alternatively, if bias is retained at either capacitor electrode, the underlay bias electrode allows for further biasing schemes.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a side view of a tunable ferro-electric gap capacitor.

FIG. 2A is a top view of a tunable ferro-electric gap capacitor.

FIG. 2B is a circuit diagram equivalent of the tunable ferro-electric gap capacitor shown in FIG. 2A.

FIG. 3 is a top view of a tunable ferro-electric gap capacitor, having a finger-like bias electrode.

FIG. 4 is a top view of a tunable ferro-electric gap capacitor, having a center portion of a bias electrode missing.

DETAILED DESCRIPTION

A tunable gap capacitor is formed on a substrate. A bias electrode is positioned between the substrate and the capacitor electrodes. Only non-conductive material is in the gap between the capacitor electrodes. Between the bias electrode and the capacitor electrodes is a FE material for tuning the capacitance of the capacitor.

In other words, only one bias electrode is introduced, as an underlay, beneath the f-e film layer deposited on the base substrate. In this

configuration, the rf electrodes provide the dc return paths for the dc bias signal. In this realization there is no need for an external dc blocking capacitor, as the dc bias introduced in this manner is inherently isolated from the rest of the circuit. A further advantage of this arrangement is that one need not increase the gap in the gap capacitor to accommodate the presence of a two layer bias electrode structure. Thus the most compact gap capacitor realization can be obtained in this manner.

The gap capacitor will now be described with reference to Fig. 1. Fig. 1 is a side view of a tunable FE capacitor 10. A substrate 12 is shown. The substrate 12 is typically a low loss ceramic material such as magnesium oxide, sapphire, or some other such similar material on which the desired f-e film can be deposited, preferably without the need for an adhesion or buffer layer. The substrate can also be a more lossy material like silicon dioxide, alumina or a printed circuit board material such as the well known material, FR4 as long as one can tolerate the added loss arising from its use, along with the added cost and complexity of using one or more buffer layers or an adhesion layer that may be necessary with these substrates.

Formed on the substrate 12 is a bias electrode 14. The bias electrode 14 is preferably doped silicon, as it can have a much lower conductivity than any metal, and its conductivity can be controlled by doping. Alternatively, the bias electrode 14 can be metal. Over the bias electrode 14 is a FE layer 16. The FE layer 16 provides the tunability to the capacitor. Over the FE layer 16 are the capacitor electrodes 21 and 24. The capacitor is part of a RF signal path. The capacitor electrodes 21 and 24 define a space between the electrodes called a gap 47. The gap 47 is defined by the electrodes. The gap 47 is shown as a dotted line. The dotted line is separated somewhat from the solid line defining the capacitor electrodes 21 and 24. This is for the sake of distinguishing between the lines defining the gap 47 and the electrodes 21 and 24, not to indicate that there is any space between the gap 47 and the electrodes 21 and 24. The gap 47 and the electrodes 21 and 24 are coterminous.

The gap capacitor will now be described with reference to Fig. 2A. Fig. 2A is a top view of the gap capacitor. A first capacitor electrode 43 and a second capacitor electrode 45 form a capacitor gap 47. A ferro-electric material 53 lies preferably underneath

the first and second capacitor electrodes 43 and 45. The ferro-electric material 53 could alternatively lie over the top of the first and second capacitor electrodes 43 and 45 assuming the proper precautions are taken to prevent the oxidation or melting of the metal traces 43 and 45 during the deposition of the f-e film on top of the electrodes. Due to these limitations, the f-e film will almost always be under the rf metal contacts, 43 and 45.

A bias electrode 55 lies preferably underneath the ferro-electric material 53. The bias electrode 55 is preferably more narrow than the ferro-electric material 53, so that the bias electrode 55 does not make electrical contact with the first or second capacitor electrodes 43 and 45.

In some cases, it may be desirable to have a bias electrode of sufficient size and electrical thickness relative to the gap region that some noticeable capacitance exists between the capacitor electrodes and the bias electrode. An example of this is in the case where the bias electrodes extends underneath the capacitor electrodes as shown in Fig. 1. In this case, the electrical equivalent circuit is shown in Fig. 2B.

In Fig. 2B, a capacitor 44 is shown coupled between two terminals 46 and 48. The capacitor 44 represents the capacitance developed between the capacitor terminals 43 and 45 of Fig. 2A. The terminals 46 and 48 represent the capacitor electrodes 43 and 45 shown in Fig. 2A. A third terminal 50 represents the bias electrode 55 shown in Fig. 2A. Two other capacitors 52 and 54 are shown coupled between the terminals 46 and 48 and the third terminal 50. The other capacitors 52 and 54 represent capacitances developed between the capacitor electrodes 43 and 45 shown in Fig. 2A and the bias electrode 55 shown in Fig. 2A.

Depending on geometry and the materials used, the capacitances of capacitors 52 and 54 may be negligible, or not, when zero volts is applied to the bias electrode 55. Also, capacitors 52 and 54 may have some non-negligible tuning characteristics, as the bias voltage applied to bias electrode 55 is varied.

Additionally, a voltage may be applied to either terminal 46 or 48, in addition to the voltage applied to terminal 50. This further modifies the tuning characteristics of the complete device shown in Fig.

2B. In other words, there are two voltage differences that can be manipulated. The two differences are (1) between terminal 46 and terminal 50 and (2) between terminal 48 and terminal 50. By varying the geometries and electrode materials different tuning characteristics can be achieved without changing FE materials and thicknesses. One drawback of the embodiment employing a bias voltage at either terminal 46 or 48 is, as already stated, that a DC blocking capacitor is then required. A DC blocking capacitor increases RF loss.

The bias electrodes need not be rectangular, as shown in Fig. 2. Preferably, the bias electrode has more than one finger as shown in Fig. 3. Alternatively, the bias electrode may have a portion removed from its center, a shown in Fig. 4. These shapes further reduce the loss introduced by the bias electrode by reducing any RF coupling to the bias electrode.

A preferred bias electrode shape will now be described with reference to Fig. 3. There are two capacitor electrodes 63 and 65 defining a gap 67. The bias electrode 80 is split into two fingers 72 and 74. A finger is defined herein as a strip thinner than the

whole object. Here it is used to mean a strip of bias electrode material thinner than the whole bias electrode. This limits the RF current that can flow in the bias electrode 70, thereby reducing the loss in the bias electrode 70. Alternatively, the bias electrode 70 may have more than two fingers (only two fingers 72 and 74 shown). Preferably, the finger width 76 is about 1 to 2 microns.

A joining member 70 connects the fingers. In another embodiment, not shown, the joining member 70 is not inside the gap 67. The figners 72 and 74 are longer and the joining member 70 is outside the gap 67 on the side where the voltage is applied. It will be understood that many variations of this shape are possible.

The bias electrode 70 is adapted to be coupled to a voltage source 78 which is coupled to a control signal generator 83. Note that the ferro-electric layer is not shown, to more clearly show the other items described.

Another bias electrode shape will now be described with reference to Fig. 4. Again, there are two capacitor electrodes 86 and 89 defining a gap 92. The

bias electrode 95 is similar in shape to the bias electrode 70 described with reference to Fig. 3. The bias electrode 95, however, has its fingers connected at the ends. In other words, the bias electrode 95 is like a rectangular bias electrode, but with its center missing. Note that the shapes of bias electrodes described with reference to Figs. 2A, 3 and 4 are simply by way of example. Other shapes, such as those having rounded corners, and asymmetrical shapes, would be within the spirit of the invention.

A variable DC voltage source 57 is coupled to the bias electrode 53 for applying a variable DC voltage to the bias electrode. Note that DC is intended to mean slowly varying with respect to a RF signal. The voltage on the capacitor electrodes will have some DC component. The DC component may be zero. The difference between the variable DC voltage applied to the bias electrode 53 and the DC component of the voltage in the capacitor electrodes 43 and 45 creates a DC electric field in the FE material 53. The variable DC voltage applied to the bias electrode 55 can be varied to change the dielectric constant of the FE material 53. This changes the capacitance of the capacitor. This changes the operating parameters of the device

incorporating the capacitor, such as, for example, a filter or a matching circuit.

A control signal generator 59 is coupled to the voltage source 57 for controlling the voltage source 57. The capacitor electrodes 43 and 45, the bias electrode 55 and the ferro-electric material 53 are all located on a substrate 61. The control signal generator 59 and the voltage source 57 may be located on the substrate 61 (as shown) or off the substrate 61 (not as shown).

The bias electrode 55 is electrically thin, preferably less than about 0.01 microns so that it is less than about 0.1 skin depths. The added rf loss arising from the presence of the bias electrode is minimal and its effect is offset by the advantage gained in fabrication and improved tuning.

The capacitor may be a tuning capacitor for use in a transceiver in a wireless communication device Preferably, the capacitor tunes a multiplexer or other filter-type device as described in U.S. Patent Application "Tunable Ferro-electric Multiplexer." The method of tuning the capacitor as described herein advantageously eliminates the need for a DC blocking

capacitor and optionally eliminates the need for a DC bias resistor.

Alternatively, the capacitor may be used in conjunction with, or as part of, a tunable matching circuit as described in U.S. Patent Application, "Tunable Matching Circuit." Again, a DC blocking capacitor and a DC resistor may be eliminated.

It will be apparent to one of ordinary skill in the art that the tunable capacitor can be used in many other electronic circuits. Such uses are within the scope of the invention.